A Distributive-Transconductance Model for Border Traps in III–V/High-k MOS Capacitors

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***Abstract*— By in-depth analysis of the electrical response of border traps in gate oxide, a new border-trap model is proposed where the ac charging and discharging current associated with those traps is proportional to the variation of the surface potential of semiconductors, resembling the behavior of transconductors. In contrast, the border trap current is directly related to the local potential in the gate oxide in the existing model. The model is then used to provide a qualitative understanding of the temperature-dependent frequency dispersion observed on the Al_2O_3/n-GaAs(111)A MOS capacitors at high positive bias.**

***Index Terms*— III–V, border trap, MOS.**

I. INTRODUCTION

III–V compound semiconductor materials have recently been identified as one of the potential candidates for post-silicon MOS technology due to their high intrinsic electron mobility [1]. However, poor interface quality often degrades the device performance. The capacitance–voltage (C–V) characteristics of III–V MOS capacitors (MOSCAPs) often show large frequency-dispersion in accumulation, i.e., the capacitance measured drops as the measurement frequency increases. It has been shown that the frequency dispersion observed in III–V MOSCAPs biased in accumulation cannot be well explained by only applying interface-trap model [2] where the trap time constant τ_{it} is given by

$$\tau_{it} = 1/(\upsilon_{\rm th}\sigma_{it} n_s) \quad (1)$$

where $\upsilon_{\rm th}$ is the carrier thermal velocity, σ_{it} is the capture cross-section, and n_s is the electron density at interface. For example, a simple calculation (using $\sigma_{it} = 1 \times 10^{-14}$ cm^2, $\upsilon_{\rm th} = 4.5 \times 10^7$ cm/s) shows that if n_s is greater than $\sim 1 \times 10^{14}$ cm^{-3}, τ_{it} will be small enough that all the interface traps should follow the measurement of ac signal in the normal frequency range (1 kHz–1 MHz) and thus no frequency dispersion is expected. However, the experimental data show considerable amount of dispersion in real accumulation [2], which calls the interface trap model into question. A model taking into account the border traps, which possess a larger time constant than interface traps, has recently been proposed to better explain the experimental data [3]. The model has already been adopted by other authors in analyzing their III–V MOS devices [4].

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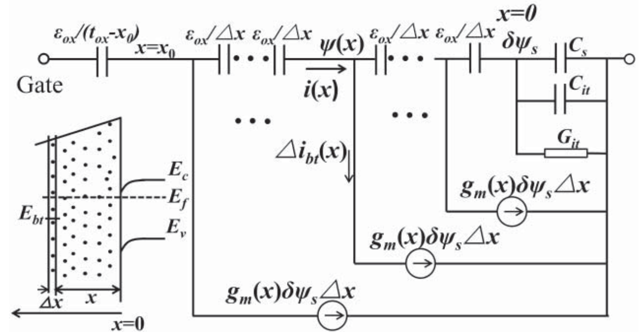

Fig. 1. Distributive transconductance model for MOSCAPs (biased in depletion or accumulation) with border traps. The lower-left inset shows a schematic band diagram of an oxide-semiconductor interface.

In this letter, we carefully analyze the ac response of border traps and derive a new electrical model. The charging current associated with border traps is identified to be controlled by semiconductor surface potential instead of the local potential inside the oxide. As an example, the model is then used to fit the temperature-dependent frequency dispersion data observed on an Al_2O_3/n-GaAs(111)A MOSCAP at positive bias.

II. DISTRIBUTIVE TRANSCONDUCTANCE MODEL FOR BORDER TRAPS

The lower left inset of Fig. 1 shows a schematic band diagram of an oxide-semiconductor interface with border traps present in oxide. According to [5], the border trap time constant at position x can be expressed by

$$\tau_{bt}(x) = \tau_0 e^{2\kappa x} \quad (2)$$

where τ_0 is the time constant at interface which equals $1/(\upsilon_{\rm th}\sigma_0 n_s)$ with σ_0 being capture cross and κ the attenuation coefficient in the electron wave function [3].

We first consider border traps at a single energy level E_{bt} (Fig. 1 inset) and assume, at thermal equilibrium, the border traps located within certain distance from the interface maintain a Fermi level the same as the semiconductor. By using similar phenomenological treatment as in [6], it can be shown that the small signal ac current flowing out of the border traps within Δx at position x can be expressed as

$$\Delta i_{bt}(x) = \frac{j\omega q f_0(1-f_0)\delta n_s N_{bt}\Delta x}{[1 + j\omega f_0 \tau_{bt}(x)]\, n_{s0}} \quad (3)$$

where $N_{bt}(x)$ (cm^{-3}) is the border-trap density at x, n_{s0} is the surface electron density at equilibrium, δn_s is the small

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signal ac component of surface electron density, and ω and f_0 are the angular frequency of the measurement signal and the Fermi distribution function for border traps at thermal equilibrium, respectively. The fact that Δi_{bt} is proportional to δn_s is because the capture rate is proportional to surface electron density. In depletion, $\delta n_s/n_{s0}$ can be expressed as

$$\delta n_s/n_{s0} = (q/kT)\,\delta\psi_s \tag{4}$$

where $\delta\psi_s$ is the small signal ac component of surface potential and T is temperature. When Fermi level is very close to conduction band minimum, the coefficient relating $\delta n_s/n_{s0}$ and $\delta\psi_s$ will be smaller than q/kT, but the essential physics does not change. By combining (3) and (4) and taking into account the energy distribution of border traps, the total charging current can be expressed as an integral

$$\Delta i_{bt}(x) = \int dE_{bt} \frac{j\omega q^2 D_{bt}(x) f_0(1-f_0)}{kT\,[1 + j\omega f_0 \tau_{bt}(x)]} \Delta x \delta\psi_s \tag{5}$$

where $N_{bt}(x)$ has been replaced by border trap density of state $D_{bt}(x)$ ($\mathrm{cm}^{-3}\cdot\ \mathrm{eV}^{-1}$). Since $f_0(1-f_0)$ is a function peaked at E_f, (5) can be approximated by

$$\Delta i_{bt}(x) = g_m(x) \Delta x \delta\psi_s \tag{6}$$

where g_m is given by

$$g_m(x) = q^2 D_{bt}(x)\left[j\frac{\arctan[\omega\tau_{bt}(x)]}{\tau_{bt}(x)} + \frac{\ln\left[1+(\omega\tau_{bt}(x))^2\right]}{2\tau_{bt}(x)} \right]. \tag{7}$$

It is clear from (6) that the contribution of border traps should be transconductance in a distributive manner. The total small-signal equivalent circuit of the MOSCAP including interface traps is shown in Fig. 1. The border trap current is controlled by the ac component of surface potential $\delta\psi_s$, whereas it is suggested to be controlled by the local potential $\psi(x)$ in [3]. Note that if $g_m(x)$ vanishes, the model returns to a normal MOSCAP with interface traps.

It should be noted that border traps that are present beyond certain distance (denoted as x_0 in Fig. 1) away from interface may not share the same Fermi level as a semiconductor at equilibrium. The physical meaning of the trap time constant is the average time that an empty trap has to wait till it catches an electron. So, it is reasonable to estimate the time constant of border traps at around x_0 to be several tens of seconds, which is the holding time commonly used before the measurement starts. Thus border traps located at and beyond x_0 cannot follow the normal measurement frequency range (1 kHz–1 MHz). As a result, they do not contribute to the total admittance although their Fermi levels are unpredictable. By careful inspection of (7), we find both the real and imaginary parts become negligibly small at x_0 compared to their maxima and decrease exponentially beyond x_0. So, it would not introduce much numerical error to set x_0 equal to the total oxide thickness t_{ox}. However, as will be discussed elsewhere, x_0 will be affected by the gate metal if t_{ox} is very small. In that case, the discussion above is not valid anymore.

Based on Fig. 1, the differential equations that determine the total ac current flow $i(x)$, and the ac potential $\psi(x)$ are

$$di(x)/dx = g_m(x)\delta\psi_s \tag{8}$$

$$d\psi(x)/dx = i(x)/(j\omega\varepsilon_{ox}) \tag{9}$$

where ε_{ox} is the dielectric constant of gate oxide. The boundary conditions are

$$i(0) = (j\omega C_s + j\omega C_{it} + G_{it})\,\delta\psi_s \tag{10}$$

$$\psi(0) = \delta\psi_s \tag{11}$$

where C_s is the semiconductor capacitance and C_{it} and G_{it} are contributions from interface traps and given in [6] as

$$C_{it} = q^2 D_{it} \arctan(\omega\tau_{it})/(\omega\tau_{it}) \tag{12}$$

$$G_{it} = q^2 D_{it} \ln\left[1 + (\omega\tau_{it})^2\right]/(2\tau_{it}) \tag{13}$$

where D_{it} ($\mathrm{eV}^{-1}\cdot\ \mathrm{cm}^{-2}$) is the interface trap density. The total admittance could be obtained by

$$Y_{tot} \equiv j\omega C_{tot} + G_{tot} = i(t_{ox})/\psi(t_{ox}) \tag{14}$$

where we have set $x_0 = t_{ox}$. Note that Y_{tot} certainly does not depend on $\delta\psi_s$.

The model derived here should be applicable to any oxide/semiconductor interface with border traps since the derivation is not material dependent. However, some parameters, such as v_{th} and κ, are material dependent and need to be calculated accordingly.

III. Results and Discussion

To get an idea of the relative contribution of border traps to the total admittance compared to that of interface traps, we calculate the magnitude ratio between total current i_{bt} that flows out of all border traps and the interface trap current i_{it} for the case of an Al_2O_3/n-GaAs MOSCAP. The current i_{bt} can be evaluated by using (8) with $i(0)$ being zeros, whereas i_{it} can be obtained by $(j\omega C_{it} + G_{it})\delta\psi_s$. The results are shown in Fig. 2. It is observed that the magnitude of i_{bt} is close to one order of magnitude smaller than i_{it} when n_s is lower than $10^9\ \mathrm{cm}^{-3}$. The ratio increases with n_s and becomes comparable to 1 at high n_s. This suggests that the effect of border traps would be more pronounced when the MOSCAP is biased close to accumulation, whereas the interface trap effect dominates when the device is more depleted. The parameters D_{bt} and D_{it} used here are $3 \times 10^{19}\ \mathrm{eV}^{-1}\cdot\ \mathrm{cm}^{-3}$ and $3 \times 10^{12}\ \mathrm{eV}^{-1}\cdot\ \mathrm{cm}^{-2}$, respectively. Those numbers are commonly observed values on many III–V MOS devices at the current stage. Note that the ratio will change accordingly if the ratio between D_{bt} and D_{it} changes since i_{bt} and i_{it} are proportional to D_{bt} and D_{it}, respectively.

GaAs MOSCAPs often show surface Fermi level pinning and the surface free electron density is very low even at high positive gate bias. Based on the observation in Fig. 2, the heavy frequency dispersion in the C-V curves observed on n-type GaAs (100), (111)B, and (110) surfaces [7] should be largely determined by interface traps, if not entirely. Recent studies [7] have shown that GaAs (111)A surface is inherently unpinned and the MOSCAP fabricated on it shows greatly improved C-V characteristics. Fig. 3(a) shows the C-V curves measured on a Ni/Al_2O_3/n-GaAs (111)A MOSCAP with the oxide thickness of 8 nm. The GaAs surface was first treated by HCL to remove the native oxide and then passivated by soaking in $(NH_4)_2S$ solution. The 8-nm Al_2O_3 was then grown on the sample by ALD followed by a post-deposition annealing at 600 °C for 30 s.

Since Fermi level at GaAs (111)A surface can be moved freely, the surface-free electron density should be high at

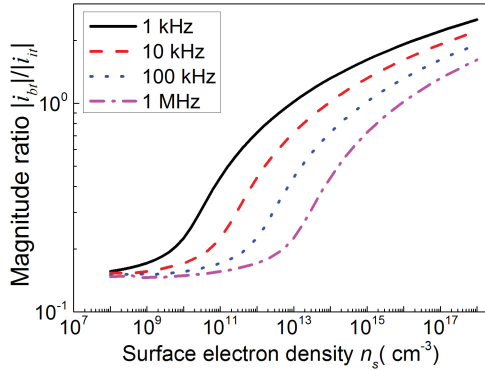

Fig. 2. Magnitude ratio between i_{bt} and i_{it} as a function of n_s. The device under consideration is an Al_2O_3/GaAs MOSCAP. D_{bt} and D_{it} used here are 3×10^{19} $eV^{-1} \cdot cm^{-3}$ and 3×10^{12} $eV^{-1} \cdot cm^{-2}$, respectively. The other parameters used are: $\kappa = 3.8$ nm^{-1}, $\sigma_{it} = \sigma_0 = 1 \times 10^{-14}$ cm^2, $\upsilon_{th} = 4.5 \times 10^7$ cm/s.

high positive gate bias. As can be seen in (12) and (13), the contribution from interface traps will be independent of frequency (1 kHz–1 MHz), and thus the residual frequency dispersion in Fig. 3(a) at high positive gate bias should be attributed to the presence of border traps.

Fig. 3(b) shows the calculated frequency dispersion of such MOS structure by using our model. The Fermi level was assumed to be 0.04 eV below the conduction band minimum and the semiconductor capacitance C_s was calculated by numerically solving Poisson's equation. D_{bt} and D_{it} used here are 6.7×10^{19} $eV^{-1} \cdot$ cm^{-3} and 6.2×10^{12} $eV^{-1} \cdot$ cm^{-2}, respectively, and the capture cross-section used is 6×10^{-15} cm^2. Other parameters are the same as used in Fig. 2. The data are taken from Fig. 3(a) at $V_g = 3$ V. Two major features of experimental data are well captured by our model. The first one is that the total capacitance decreases roughly linearly with respect to the logarithm of measurement frequency, and the amount of frequency dispersion in terms of F/decade does not change much with temperature. The other is that the absolute value of total capacitance decreases at low temperature. In fact, the parameter that is found to be sensitive to temperature in our calculation is the surface electron density. It decreases with the decrease of temperature and thus leads to an increase of border-trap constants at low temperature. Since what determines the behavior of traps is essentially the product $\omega\tau$, the increase of τ will make the entire calculated curve move to the left, which is seen in Fig. 3(b).

To further verify our model, we have fitted the experimental capacitance and conductance data for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP in [3] with excellent agreement, by using a border trap density of 1.85×10^{19} eV^{-1} cm^{-3} and interface trap density of 2.45×10^{12} eV^{-1} cm^{-2}. The parameters κ and υ_{th} are calculated to be 5.1 nm^{-1} and 5.8×10^7 cm/s, respectively, for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ system. The capture cross-section used is the same as that in Fig. 3, and the semiconductor capacitance C_s is calculated to be 9.5 fF/μm^2 assuming Fermi level is at the conduction band minimum.

In summary, we have presented a new electrical model for border traps where the charging current is controlled by the surface potential of the semiconductor. It differs from the previous model where the current is controlled by the local potential in oxide. This letter should help advance the understanding of nanowire-based MOSFETs especially given the multiple facets of different crystal orientations present.

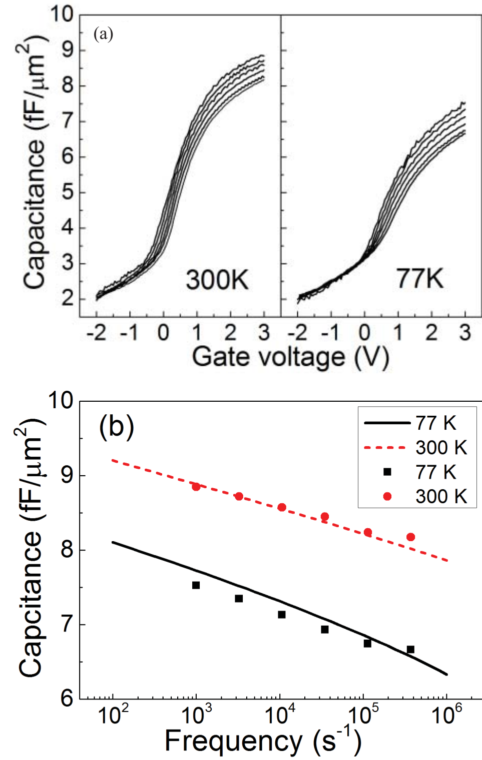

Fig. 3. (a) C-V characteristics of a Ni/8nm-Al_2O_3/n-GaAs(111)A MOSCAP measured at 300 K and 77 K. The frequency ranges from 1 kHz to 373 kHz with uniform spacing in log scale. (b) Frequency dispersion calculated by using our model (line) and experimental data taken at $V_g = 3$ V (dots). The Fermi level was assumed to be 0.04 eV below the conduction band minimum. D_{bt} and D_{it} used here are 6.7×10^{19} $eV^{-1} \cdot cm^{-3}$ and 6.2×10^{12} $eV^{-1} \cdot$ cm^{-2}, respectively. The capture cross-section used is 6×10^{-15} cm^2. Other parameters are the same as in Fig. 2.

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