Flexible Vertical Light Emitting Diodes

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Recently developed concepts in materials, manufacturing approaches and mechanics strategies open up opportunities for building optoelectronic systems with high performance, inorganic semiconductors in systems that afford exceptional levels of mechanical deformability (e.g., ability to bend and stretch), diversity in geometric layouts (e.g., large-area coverage, in dense or sparse coverages), and versatility in substrate choices (e.g., plastic, rubber). Each of these capabilities offers options in engineering design that are not easily addressed with conventional, wafer-based devices.[1–6] Some of the most successful demonstrations involve top-down methods to define and release structures of active materials (or fully/partially formed devices) in ultrathin, microscale configurations from wafer hosts where they are deposited, grown and/or processed. Selective etching of a buried, sacrificial layer often enables this release, in schemes that use the techniques of transfer printing as routes to deterministic assembly on substrates of interest.[7–9] Key issues include, among others, (1) release layers and etching chemistries that do not degrade the active materials, (2) designs in structures (i.e. anchors) that tether released materials/devices to their lithographically defined locations, but that easily fracture during transfer printing and (3) schemes for interconnecting the materials/devices after their assembly on a target substrate. The present work presents two new concepts: the first addresses topics of relevance to (2), in a way that significantly relaxes requirements to achieve (1); the second relates to (3). Specifically, we propose and demonstrate engineering designs and materials that not only tether the materials/devices to the host substrate, but also simultaneously prevent their exposure to etchants applied during the release process. Further, an advanced interconnection scheme and vertical device layout facilitate electrical contacts and system integration. These two ideas are demonstrated with red emitting microscale light emitting diodes(μ-ILEDs) based on AlInGaP, both as individual devices and as interconnected arrays, on substrates ranging from glass to plastic. Comparisons to behaviors of devices formed using previous approaches illustrate the value of these techniques, both in performance and in integration schemes.[10]

Thin epitaxial layers in stacks that consist of a p-spreading layer ($Al_{0.45}Ga_{0.55}As$:C)/p-cladding layer ($In_{0.5}Al_{0.5}P$:Zn)/quantum well ($Al_{0.25}Ga_{0.25}In_{0.5}P$/$In_{0.56}Ga_{0.44}P$/$Al_{0.25}Ga_{0.25}In_{0.5}P$)/n-cladding ($In_{0.5}Al_{0.5}P$:Si)/n-spreading layer ($Al_{0.45}Ga_{0.55}As$:Si)/n-GaAs:Si, grown on a 500 nm thick sacrificial layer of $Al_{0.96}Ga_{0.04}As$ on a GaAs wafer serve as active materials. This design allows selective elimination of the sacrificial layer with hydrofluoric (HF) acid, to release arrays of individual, ultrathin, microscale devices (i.e. μ-ILEDs) from the underlying growth substrate.[11] **Figure 1** illustrates key steps for fabricating these μ-ILEDs in procedures that isolate the active layers from the processing, to avoid any degradation in performance. The schematic illustration and scanning electron microscope (SEM) image in Figure 1a, collected after a dual etching process (see experimental section), show isolated μ-ILEDs on the wafer, with etched relief to expose mesa regions of n-GaAs for contacts, and the perimeter sidewalls of the sacrificial layers. In this example, the devices have lateral dimensions of 140×140 μm^2 (dimension of p-GaAs region = 80×80 μm^2, covered by a hard mask of SiO_2), and the exposed n-GaAs mesa regions extend 30 μm beyond their edges. Next, photolithography defines patterns of photoresist that encapsulate the μ-ILEDs, to protect the active layers and their sidewalls (from the top SiO_2 mask to

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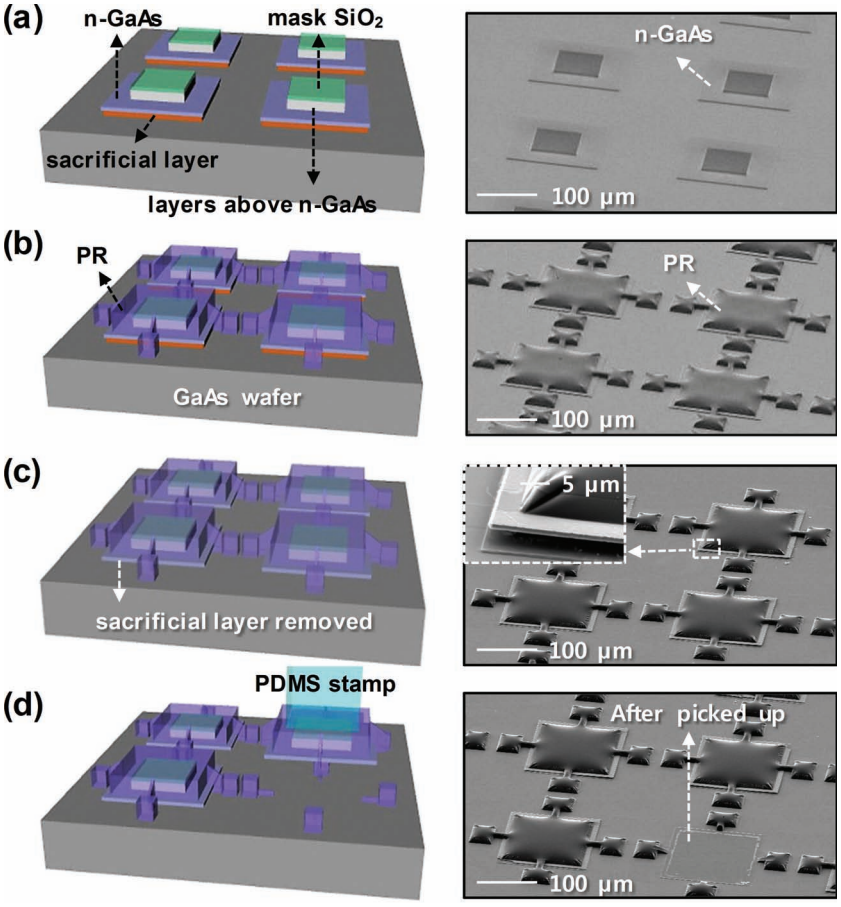

Figure 1. Schematic illustrations and SEM images corresponding to the main process steps for defining, releasing and transfer printing μ-ILEDs, in a way that retains pristine active layers and enables backside contacts. The frames correspond to the status after (a) lateral delineation of devices on a wafer, (b) formation of protective anchors around isolated μ-ILEDs, (c) removal of the sacrificial layer, and (d) selective retrieval selected μ-ILEDs. The SEM image in the inset of the right frame (c) shows devices after removal of the sacrificial layer.

the bottom n-spreading layers) from immersion in HF, but with the sacrificial layers exposed for subsequent undercut etching (Figure 1b). This configuration is important because it addresses difficulties associated with the propensity for the cladding layers, in particular, to be etched slightly when in contact with HF. These patterns of photoresist also mechanically anchor the μ-ILEDs to the underlying wafer after removal of the sacrificial layers. As a result, we refer to these patterns as protective anchors, to distinguish the designs from similar, previous ones that provide only the anchoring function.[11] Immersion in dilute HF releases isolated μ-ILEDs, as shown in the schematic illustration and SEM image of Figure 1c. These steps prepare the devices for deterministic assembly using the techniques of transfer printing.[12] Here, the protective anchors fracture to enable high yield retrieval onto the surfaces of soft, elastomeric stamps with matching features of relief. Figure 1d shows a region of a substrate after removal of one device (see also Figure S1a-c).

To highlight a key advantage of this scheme, **Figure 2** a presents a tilted view SEM image of a transfer printed μ-ILED (100×100 μm^2) formed using a simple, non-protective anchor. The results reveal that the p and n-cladding layers ($In_{0.5}Al_{0.5}P$) above and below the quantum well are etched slightly (roughly ~4.3 μm laterally; see bottom frame of Figure 2a), while layers with Al content ≤ 0.45 are unaffected. The data of Figure 2b show that the etch rates of the sacrificial and cladding layers are 0.84 μm/min and 0.023 μm/min, respectively. The former suggests a minimum undercut etching time of ~60 minutes in the diluted HF solution, for μ-ILEDs with dimensions of 100×100 μm^2. During this time, the expected lateral etch distance of the cladding layer is ~1.5 μm. (The results of Figure 2a used etching times of ~180 minutes to amplify the effects.) Even moderate etching of the cladding layers can lead to undesirable effects on performance. Current-voltage (I-V) measurements on transfer printed μ-ILEDs with different dimensions (ohmic p- (Pt/Ti/Pt/Au, 10/40/40/70 nm) and n- (Pd/Ge/Au, 5/35/70 nm) type contacts) reveal that damage in the cladding layers leads to increased turn-on voltages (Figure 2c). Observed increases in the magnitude of this effect with decreasing lateral dimensions in the devices suggest edge related effects, likely due to enhanced series resistances associated with elimination of the cladding layers and/or generation of lattice defects and dangling bonds at the exposed sidewall surfaces.[13] Large devices (e.g. 200×200 μm^2) exhibit turn-on voltages similar to those of otherwise similar counterparts that have not been exposed to HF (Figure S2).

A set of μ-ILEDs fabricated with protective anchors appears in Figure 2d, in a procedure that follows steps described in Figure 1 but enables fully formed device formats with ohmic contacts. Microscope images in the top and bottom frames correspond to μ-ILEDs with protective anchors on a GaAs wafer and transfer printed on a PDMS substrate, respectively (see Figure S3 for the alternative method). Figure 2e and S3b present I-V characteristics of a set of such devices before and after release/printing. The I-V characteristics are almost identical, indicating absence of any damage associated with processing. The associated optical output powers are also superior to those of devices processed with non-protective anchors, as shown in Figure 2f. The strong decreases in output intensity at 2.5 mA, for example, are not observed in otherwise similar devices before undercut etching, or in those fully processed and transfer printed using protective anchors. The broader trend of reduced optical output intensity for driving currents of 7.1 mA is associated with cumulative heating due to poor heat dissipation on the glass substrate.[14]

By comparison to the top, lateral configuration of contacts used in the devices of Figure 2, a scheme in which the bottom contact extends across the entire device is preferred because it reduces current crowding at high forward injection current, and improves reliability and lifetime. In this

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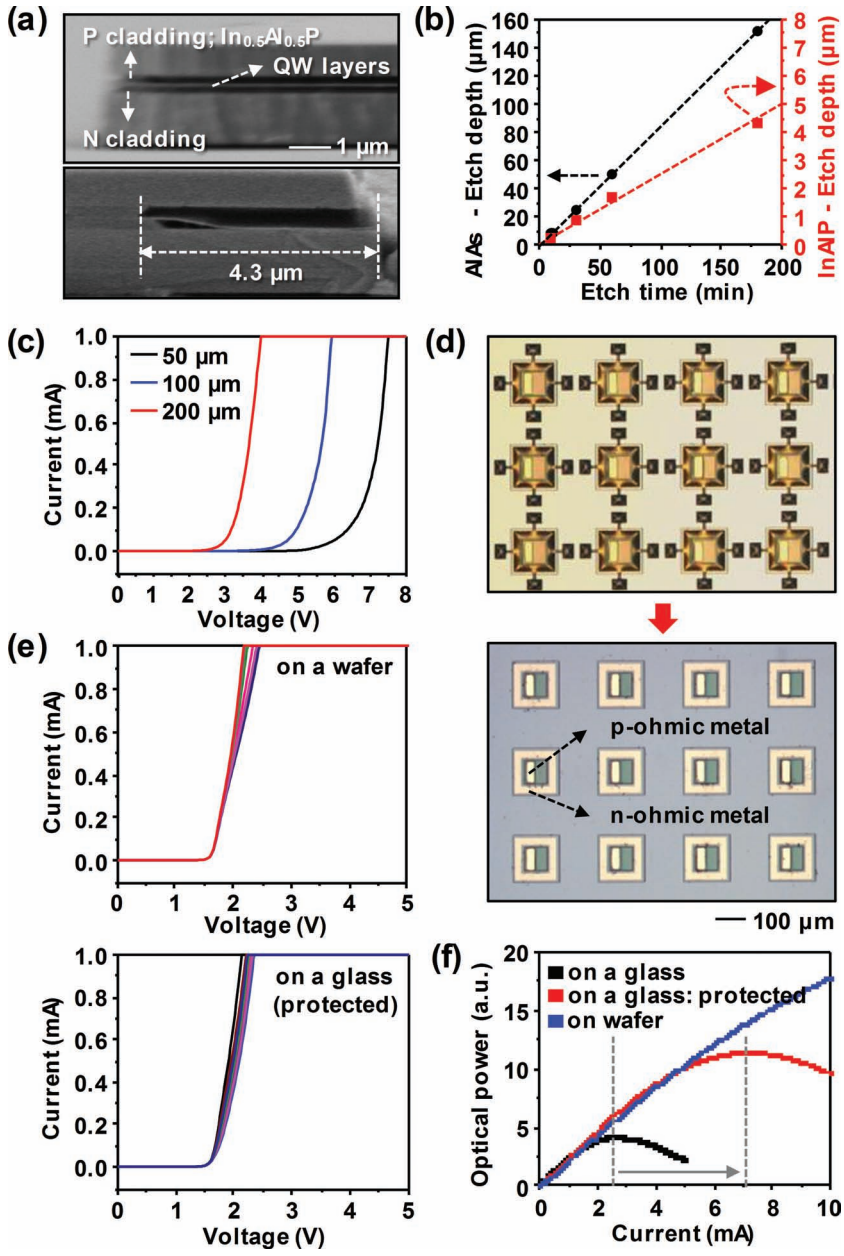

Figure 2. (a) Tilted view SEM image of a transfer printed μ-ILED formed with a simple, non-protective anchor scheme. (b) Lateral etching rate for $Al_{0.96}As_{0.04}$ sacrificial and $Al_{0.5}In_{0.5}P$ cladding layers. (c) Current-voltage (I-V) characteristics for μ-ILEDs with different dimensions, formed with non-protective anchors. (d) Microscope images of a set of fully formed μ-ILED before and after transfer printing. In the left image, both p- and n-type ohmic metal contacts were formed before defining protective anchors and subsequent undercut etching. The image in the right frame shows μ-ILEDs after transfer printing and removal of protective anchors by acetone. (e) Current-voltage characteristics of a set of μ-ILEDs, fabricated on a wafer (top frame) with protective anchors and then transfer printed onto a glass substrate with an adhesive layer coating (epoxy, bottom frame). (f) Relative optical output power as a function of driving current for three different cases: on the source wafer before release, on the target substrate after release for devices processed with non-protective and protective anchors.

context, the protective anchor scheme and terraced shape of device have an additional advantage: they allow a simple method to generate μ-ILEDs with contacts across the entire base areas of the device, while they are on the transfer stamp. **Figure 3**a-c provides schematic illustrations (left frame) and microscope images (right frame) of this concept. After retrieving a collection of μ-ILEDs with a PDMS stamp (flat slab geometry shown here) from a GaAs wafer (Figure 3a), the exposed n-GaAs can be partially removed by immersion in a wet etchant (H_3PO_4: H_2O_2: D.I. = 1: 13: 12) that does not affect other active layers of the devices, due to their encapsulation by the remaining parts of the protective anchors. Next, electron beam evaporation of uniform layers of Pd/Ge/Au (5/35/70 nm) forms ohmic contacts to the n-GaAs as shown in 3b. The wrinkling corresponds to buckling that occurs in the bare regions of PDMS due to mismatches in the thermal expansion coefficients of the metallization and the PDMS.[15] The schematic illustration and micrograph in Figure 3c and the SEM image in Figure S4a show the surface of the PDMS after transfer printing; only the μ-ILEDs, with integrated n-type ohmic contacts, transfer and not the metal deposits in the intervening regions on the PDMS. The step height associated with the μ-ILEDs and the protective anchors, along with a shadowing effect in the evaporation (Figure S4b), prevent deposition of metal onto the edges of the active layers, as shown in the SEM image of Figure 3d. A microscope image of transfer printed μ-ILEDs with backside contacts on a glass substrate coated with the adhesive layer of epoxy (SU8_2) appears in Figure 3e. The inset micrograph highlights the backsides of these devices integrated on a transparent substrate, with deposited backside metal layers (i.e. bottom electrodes).

The schematic illustration in **Figure 4** a presents the device configuration that results from the procedure described in Figure 3. After transfer printing, the thin n-GaAs layer can be etched away to expose the bottom ohmic metal, in a scheme where a top layer of Pd serves as an etch stop. A microscope image of a set of resulting devices after separate formation of p-type ohmic metal contacts on p-GaAs (following removal of the layer of SiO_2) appears in Figure 4b. Figure 4c presents the luminance-current-voltage (L-I-V) characteristics of a representative device in a vertical configuration with different n-GaAs thicknesses, achieved by changing the duration of the etching process outlined in Figure 3a. This thickness affects the transmission of light reflected upward by the backside n-type ohmic metal. As expected, the optical output power increases with decreasing n-GaAs thickness; the I-V characteristics do not change substantially but monotonic increases in series resistance are noted, due to increases in ohmic losses through

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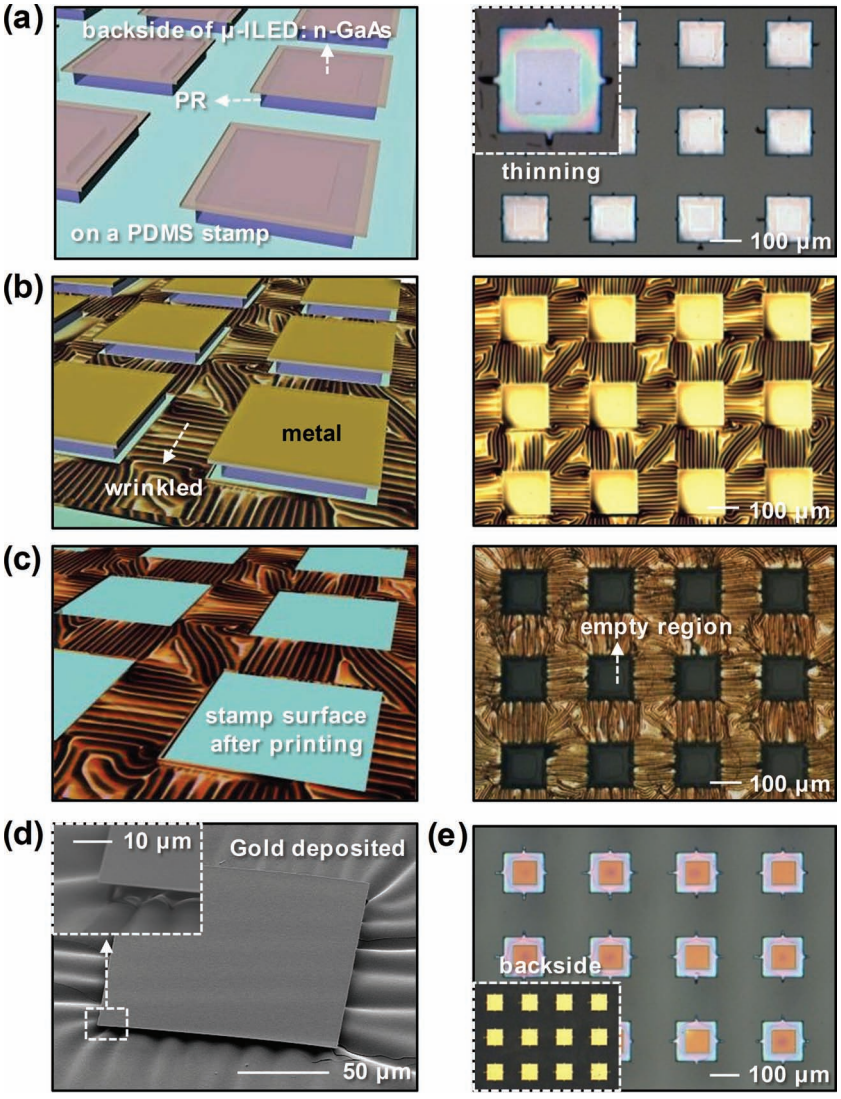

Figure 3. (a)-(c) Schematic illustrations and microscope images of key process steps for generating vertical device configurations, using a modified version of the process in Figure 1. The frames show the sample status after (a) retrieval of a set of μ-ILEDs, (b) selective deposition of metal layers on their back surfaces, and (c) transfer printing, respectively. The inset microscope image in the right frame of (a) shows the back of the device after thinning the n-GaAs. (d) SEM image after deposition of metal layers. The inset presents a magnified view of the sidewall of the device, showing discontinuity in the metal film. (e) Microscope images of a set of μ-ILEDs after transfer printing on a glass substrate with an adhesive layer (epoxy), prepared via the fabrication procedure described in frames (a-c). The inset highlights the metal deposited onto the backsides of the devices.

the n-GaAs layers. Re-plotting the results reveals an exponential increase in output power with decrease in the thickness of the n-GaAs (Figure 4d, red circles), with a total of ~36% enhanced power at a thickness of 50 nm. The calculated reflectance values for five different n-GaAs layer thicknesses (from 50 to 450 nm with a 100 nm step) at a wavelength of 670 nm are also shown in Figure 4d (blue circles). The full spectral responses appear in Figure S5. Here, a 100 nm thick layer of Au is used in the simulations, which yield results that are consistent with improved reflection from the bottom Au metal as the thickness of n-GaAs layer decreases.

These vertical μ-ILEDs can be built into systems by using thin film processing steps reported elsewhere.[16] Here, spin casting a thin dielectric layer (epoxy; SU-8; 1.2 μm thickness) with patterned openings at the p- and n-type ohmic contacts and establishing metal interconnects to transfer printed μ-ILEDs yields interconnected array geometries. Optical images of a 5 × 5 array are provided in Figure 4e. A thin sheet of polyethylene terephthalate (PET; Grafix DURA-RAR, 50 μm thickness) serves as the substrate, shown wrapped around a glass cylinder (Inset shows this array in a flat state). Each row is composed of five μ-ILEDs connected in series, with rows connected in parallel. The uniform emission characteristics at various operation currents (1 ~ 4 mA) indicate that all μ-ILEDs have similar contact resistances and properties (see Figure S6). The results in Figure 4f show invariant I-V characteristics with bending deformations.

Another means to exploit the backside metal contact involves interconnection geometries in which the devices are bonded, electrically and mechanically, to prepatterned electrodes on the receiving substrate. Here, cold welding of gold to gold provides an attractive option, facilitated by the ability of the elastomeric stamp to provide conformal contact between the metalized bottom surfaces of μ-ILEDs and thin film metal traces on a receiving substrate.[17,18] Figure 4g shows a schematic, exploded view illustration and optical image, respectively, for an addressable 11 × 11 array of μ-ILEDs on a thin sheet of PET film, to demonstrate this concept. A bilayer of Cr/Au (30/500 nm) on the PET substrate cold-welds (<100 °C, ~100 kPa) to the backside metal on the devices. The relatively mild conditions avoid mechanical damage or chemical transformation of the PR protective anchors, and enable facile removal of PR, after the cold-welding process, with acetone. Various images of operating 11 × 11 arrays appear in the right frame of Figure 4g and Figure S7 (The I-V characteristics appear in Figure S8).

The results presented here establish simple materials and engineering schemes that enhance significantly the performance and integration possibilities for inorganic optoelectronics on unusual substrates. The same procedures and strategies should also be applicable to other classes of components, with complex active layers and materials other than those illustrated here.

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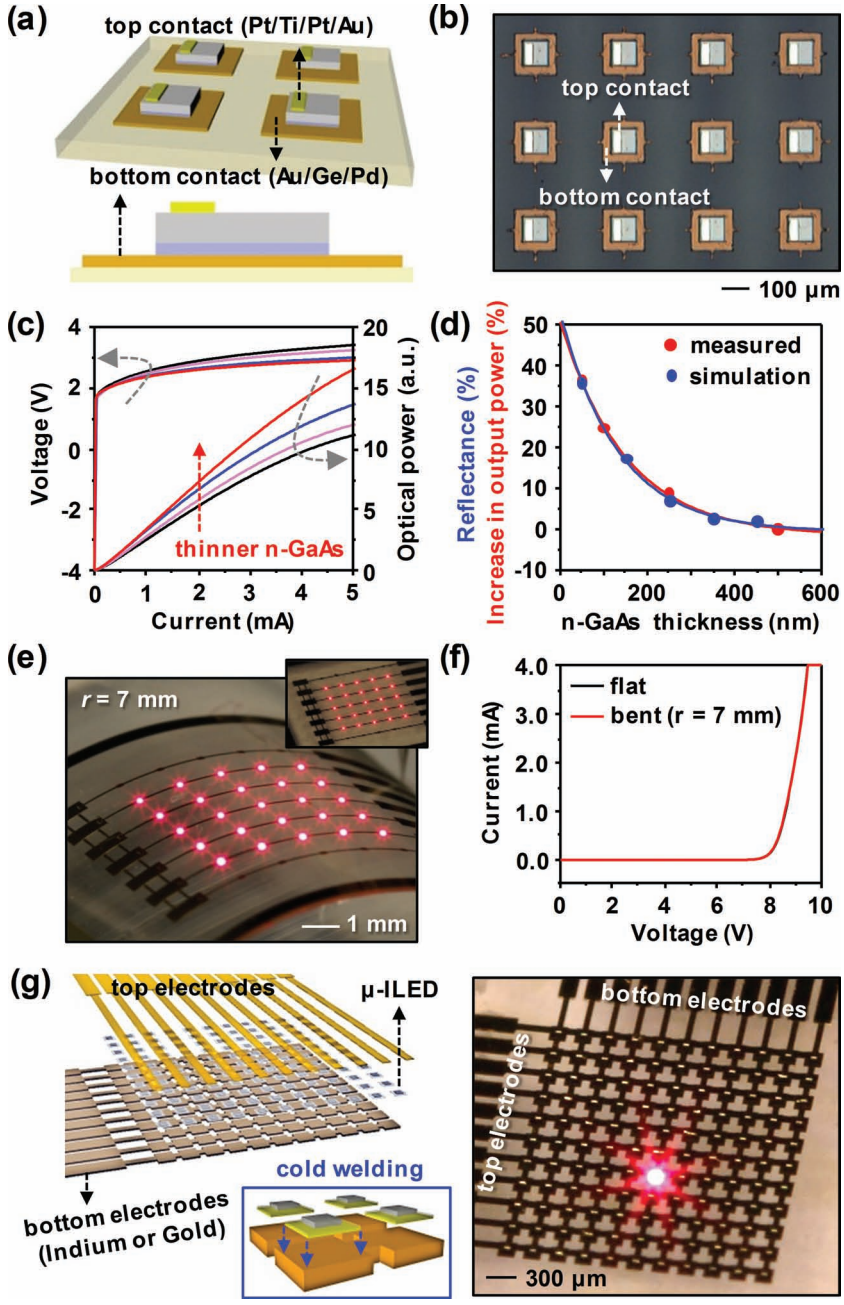

Figure 4. (a) Tilted (top frame) and cross sectional (bottom frame) view schematic illustrations of the vertical device configuration, respectively. (b) Microscope image of a set of μ-ILEDs in a vertical configuration, after transfer printing onto an epoxy-coated glass substrate. (c) Luminance-current-voltage (L-I-V) measurements with different n-GaAs thicknesses. (d) Re-plotting of data in (c) as a function of n-GaAs thickness (red circles), where the optical output intensities correspond to operating currents of 2 mA. The computed (RCWA) reflectance values also appear as a function of n-GaAs thickness at the wavelength of 670 nm (blue circles). (e) Optical images of a 5 × 5 array of μ-ILEDs with a vertical configuration in a bent state (bending radius = 7 mm) and in a flat state (inset micrograph). Each row is composed of five μ-ILEDs connected in series; the rows are connected in parallel. The driving current is 3 mA for both cases. (f) Current-voltage characteristics of the array shown in (e)e in flat and bent states, respectively (current compliance = 4 mA). (g) Exploded schematic illustration and representative optical image showing an array of vertical μ-ILEDs, generated via a cold-welding process.

Experimental Section

Fabrication of AlGaInP μ-ILEDs with protective anchors: The process began with photopatterning a hard mask of SiO_2 followed by inductively coupled plasma reactive ion etching (ICP-RIE, $Cl_2/H_2/Ar$ = 4/2/4 sccm, pressure = 2 mTorr, plasma power = 100 W, inductor power = 500 W), and then wet etching with H_3PO_4: H_2O_2: D.I. = 1: 13: 12. Patterns of photoresist formed protective anchors around the isolated structures that resulted from these etching procedures. The photolithography used photoresist (PR; SPR220_3.0) spin-cast at 3000 rpm for 30 seconds, soft-baked at 110 °C for 60 seconds, exposed to ultraviolet (UV) light at a dose of 25 mW/cm^2 and then developed (MF24A developer) for 90 seconds and baked at 130 °C for 10 minutes.

Transfer Printing: Casting and curing a pre-polymer to PDMS (Sylgard 184, Dow Corning, 10:1 mixture of pre-polymer to curing agent) against a pattern of a negative photoresist (SU8_50, MicroChem., 100 μm thickness) on a Si wafer formed PDMS stamps with features of relief (100 × 100 μm^2 posts) designed for selective transfer printing, as shown in Figure 1d.

Fabrication of vertical light emitting diodes (VLEDs): Electron beam evaporation of Pd/Ge/Au (5/35/70 nm) directly on the backsides of μ-ILEDs with protective anchors after retrieval with a PDMS stamp formed n-type ohmic contacts. Transfer printing delivered the resulting μ-ILEDs onto substrates of interest, often coated with a thin (~1.2 μm) layer of semiconductor-grade epoxy (SU8) as an adhesive. Photolithography (AZ5214 PR) and lift-off defined patterns of p-type ohmic metal (Pt/Ti/Pt/Au, 10/40/40/80) in the regions of exposed p-GaAs after removal of both the PR and remaining SiO_2 mask with acetone and buffered oxide etchant (6:1 BOE for 30 seconds), respectively. For the array layout in Figure 4e, a thin photopatterned layer of epoxy exposed both the p- and n-type ohmic metals to provide electrical isolation. Finally, patterning metal interconnects formed by sputter deposition (Cr/Au, 30/300 nm) and defining another encapsulating layer of epoxy by spin casting completed the procedure.

Reflectance spectra calculation: Reflectance spectra of vertical μ-ILEDs with different n-GaAs layer thicknesses were calculated by using the rigorous coupled-wave analysis (RCWA) (DiffractMod 3.1, RSoft Design Group, USA). To remove effects of surface reflection, the longitudinal spatial domain was defined to span the p-spreading layer and the Au metal layer. For simplicity, the n-metal layer was approximated as a single layer of Au. The refractive indices and absorption coefficients of each material were taken from the literature.[19–22]

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Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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